Transparent and Flexible Graphene Charge-Trap Memory

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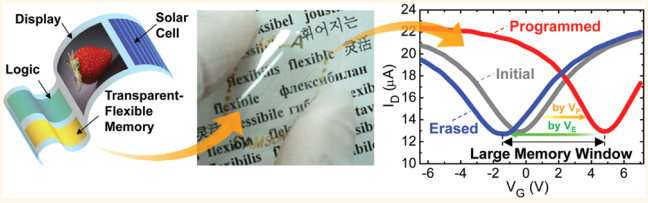
ABSTRACT



A transparent and flexible graphene charge-trap memory (GCTM) composed of a single-layer graphene channel and a 3-dimensional gate stack was fabricated on a polyethylene naphtalate substrate below eutectic temperatures (~110 °C). The GCTM exhibits memory functionality of ~8.6 V memory window and 30% data retention per 10 years, while maintaining ~80% of transparency in the visible wavelength. Under both tensile and compressive stress, the GCTM shows minimal effect on the program/erase states and the on-state current. This can be utilized for transparent and flexible electronics that require integration of logic, memory, and display on a single substrate with high transparency and endurance under flex.

KEYWORDS: graphene · nonvolatile memory · charge-trap memory · transparent · flexible

Electronic modules have been going through extensive renovations in order to incorporate multiple functionalities, such as portability, transparency, flexibility, and wearability. This would require multiple core electronic devices, such as logic, memory, and display to be integrated on a single transparent-flexible substrate without degrading the transparency from the addition of active layers and device performance under flex. In the past decade, difficulties in achieving transparent high-quality crystalline inorganic materials on transparent-flexible substrates have made organic materials[1,2] and semiconducting nanowires[3,4]/nanotubes[5,6] favorable for transparent-flexible electronic devices.[7,8]

Alternatively, the two-dimensional graphene can offer enhanced performance to transparent-flexible electronic modules because it inherently possesses high carrier mobility[9] with minimal light absorbance.[10] Furthermore, due to the strong hexagonal covalent bonds, graphene maintains its extraordinary mechanical properties even at the nanoscale regime.[11] In recent years, the success of artificially growing large scale graphene[12,13] has led to graphene-based transparent electrodes,[10] which transcended to the emergence of graphene-based touch screen, liquid crystal display, organic solar cells, and organic light emitting diodes. In addition to graphene being exploited as a passive element, flexible and stretchable graphene transistors have also been demonstrated using an ion-gel gate dielectric.[14,15]

The single atomic profile and the astonishing physical properties of graphene can also allow advancements in a variety of memory metrics when implemented into several types of memory architectures. For example, in recent years, various types of graphene-based memory devices have been demonstrated; for example, a flash memory with graphene floating-gate,[16] ferroelectric memories with graphene channel,[17,18] charge-trap memories using dielectric stacks on graphene channel,[19,20] resistive memories using reduced graphene-oxide,[21,22] and nanoelectromechanical switches using graphene beams.[23,24] In addition, by integrating graphene with polymers and/or flexible substrates,[25−28] a spectrum of graphene-based memory applications is streaming toward transparent flexible- and wearable-electronics. Transparent-flexible memory modules, however, have been limited to memristive systems.

In this paper, we show memory operation in transparent-flexible graphene charge-trap memory (GCTM) devices that are fabricated on a transparent-flexible polyethylene naphthalate (PEN) substrate. The GCTM is composed of a single-layer graphene channel field-effect transistor with a triple high-*k* dielectric ($Al_2O_3/HfO_x/Al_2O_3$) gate-oxide stack.

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Received for review May 18, 2012 and accepted August 13, 2012.

Published online August 13, 2012
10.1021/nn302193q

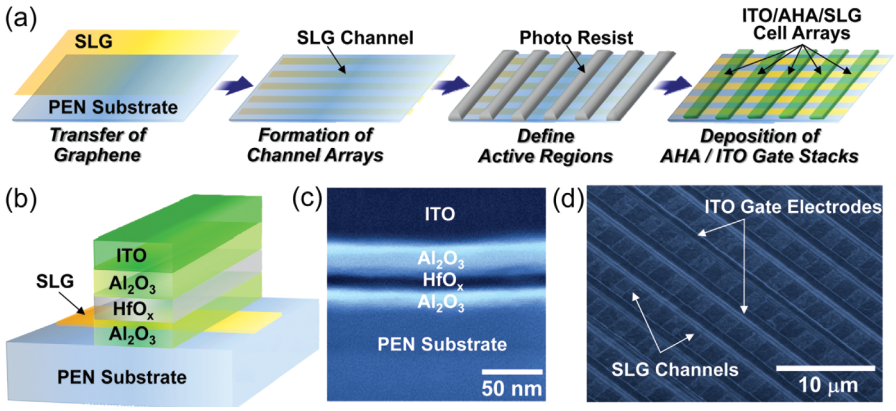

Figure 1. (a) Fabrication process steps of transparent-flexible GCTM. (b) Schematic illustration of GCTM device structure. (c) Cross-sectional TEM image of $Al_2O_3/HfO_x/Al_2O_3$ (AHA) gate stack in GCTM. (d) Bird's eye view SEM image of high-density GCTM array.

Although the memory performance can be characterized through many means, we focus on the degradation of transparency due to the active graphene/triple-gate stack, the operating mechanism, and retention properties of the memory function, and the influence of bending stress on the device performance.

RESULTS AND DISCUSSION

Most transparent-flexible substrates cannot withstand high temperatures associated with processing steps necessary for device fabrication due to the low glass transition and/or thermal decomposition temperatures of the substrate. An advantage in using graphene as an active layer is to eliminate high temperature processes that are generally required for obtaining high quality channel materials and Ohmic source/drain junctions. Here, we fabricate the transparent-flexible GCTM through a multistep procedure at temperatures below 110 °C as shown in Figure 1a. First, single-layer graphene was grown on a copper film by plasma-enhanced chemical vapor deposition (CVD),[16,29] transferred onto a PEN substrate, and characterized through Raman spectroscopy (see Supporting Information).[16,17,20,29,30] Active channel regions were then patterned by photolithography and etched through oxygen plasma. Next, a photoresist mask was formed by photolithography and a thin Al layer of 12 Å was deposited and oxidized in air to promote nucleation of Al_2O_3.[16,31] Finally, a triple-gate stack of $Al_2O_3/HfO_x/Al_2O_3$ (8 nm/8 nm/25 nm) was subsequently deposited through atomic layer deposition, and transparent indium tin oxide (ITO) gate electrodes were formed by sputtering and lift-off. The schematic diagram, cross-sectional transmission electron microscope (TEM) image of the as fabricated GCTM, and scanning electron microscope (SEM) image of the high-density GCTM array are shown in Figure 1b–d. The triple gate stack comprising an Al_2O_3 tunnel oxide, a HfO_x charge trap layer, and an Al_2O_3 control oxide is clearly noticeable. The SEM image of the array (Figure 1d) is to demonstrate a possible cell circuitry composed of GCTMs without metal electrodes. The semimetallic property of graphene allows the graphene to be used as either the channel material or the interconnections. In other words, the region of graphene underneath the gate stack serves as the channel material, while the rest of graphene may function as both the source/drain contacts and interconnections.

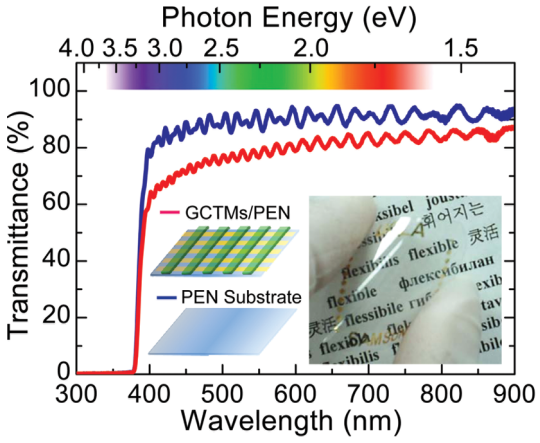

Figure 2. Optical transmittance spectra of GCTM and PEN substrate. The addition of GCTM on the PEN results in an 8% reduction of transparency in the visible wavelengths. (Inset) Photograph of the transparent-flexible GCTM array fabricated on PEN.

We first examine the transparency degradation arising from the addition of GCTM on the PEN substrate. Figure 2 compares the optical transmittance spectra of the PEN substrate with and without the GCTM array. The active layers reduce the transparency only by 8% in the visible-infrared wavelength range (400–900 nm) and sustain its transparency without distorting an image behind the GCTM array (inset of Figure 2). Minimum requirement for transparency for an active electronic element should be greater than 80% considering the transparency of a transparent electrode is nowadays above 90%.[32] Up to date, transparency ranging in 60–80% has been demonstrated in various transparent electronic modules; for example, semiconducting nanowires/nanotube transistors and logic gates (>80%),[4,5,33,34] wide bandgap transparent conducting oxide memory structures (~80%),[35] organic light emitting diodes (~70%),[36] and grid structured lithium-ion batteries (~60%).[37] Our GCTM array shows transmittance over

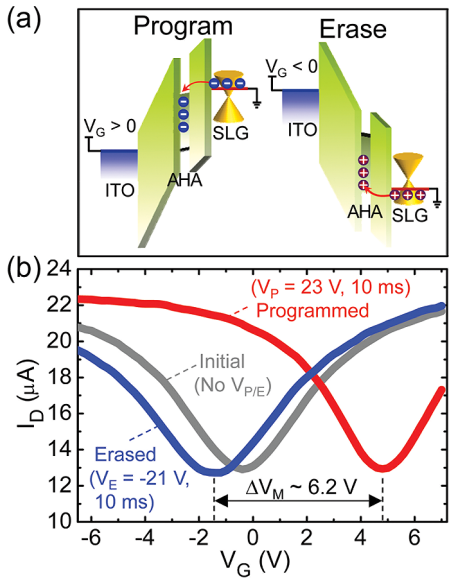

Figure 3. Operation mechanism of GCTM. (a) Band diagram of GCTM across the gate stack. The program and erase operation are based on electron and hole injection, which depends on the polarity of the gate voltage. (b) Typical memory functions of GCTM in air at V_D = 1 V. The device shows a shift of Dirac point under gate voltage stress.

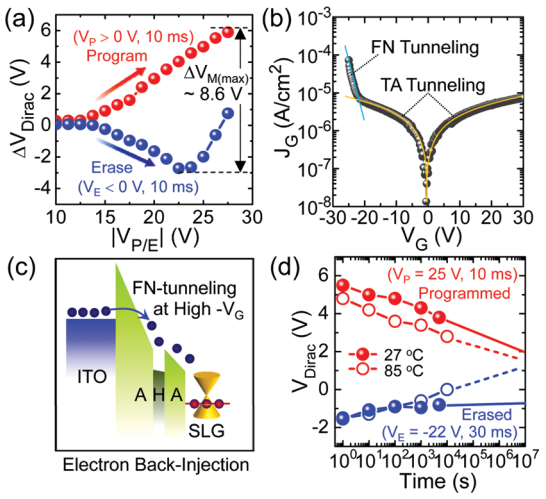

Figure 4. Electrical characteristics in air of GCTM. (a) Memory window as a function of program/erase voltage. A maximum window of ~8.6 V is achieved. Electron back injection starts to occur at erase voltage of *ca.* -22 V. (b) Gate tunneling current density. The tunneling mechanism for the standard program/erase operation corresponds to trap-assisted (TA) tunneling and the electron-back injection arises through Fowler–Nordheim (FN) tunneling. (c) Illustration of the electron back-injection mechanism associated with Fowler–Nordheim tunneling. (d) Retention characteristics of GCTM. For all of the measurements, V_D was fixed at 1 V.

80% in the visible-infrared regions, which is comparable to the most transparent active components.

Next, we study the electrical performance of the GCTM where all electrical measurements were taken on individual GCTM devices with channel dimensions ($W/L \approx 4.5\ \mu m/30\ \mu m$) and Ti/Al (10 nm/100 nm) source/drain contacts due to the difficulties in probing the monolayer graphene electrodes. The operational mechanism of the program/erase mode in our GCTM is illustrated in Figure 3a, where the energy band diagrams were represented on the basis of the Anderson model[38] (see Supporting Information). In the program (erase) mode, where the gate is under a positive (negative) voltage, the internal electric-field within the gate stack and the thin Al_2O_3 tunneling oxide permits electrons (holes) from the graphene to be injected into the HfO_x charge trap layer. The trapped electrons (holes) effectively dope the graphene to p-type (n-type) and results in a positive (negative) shift of V_{Dirac}. This is shown in Figure 3b, where a positive (negative) shift of V_{Dirac} occurs upon applying a program (erase) voltage pulse of V_P = 23 V ($V_E = -21$ V). The trapped charges in the charge trap layer modify the energy band alignment of the gate stack and lead to a memory effect in the device characteristics. The change of the electrochemical potential within the gate stack leads to the shift of the Dirac point (ΔV_{Dirac}), from which the memory window (ΔV_M) of the GCTM can be defined.

The memory window of charge-trap memories is determined by the number of trapped charges in the charge storage layer, which rely on the magnitude of program/erase voltages. Thus, we examine the ΔV_{Dirac} at various magnitudes of $|V_{P/E}|$. As shown in Figure 4a, the memory effect starts at a voltage pulse of $|V_{P/E}| \approx 14$ V and increases monotonically as $|V_{P/E}|$ increases, resulting in a maximum memory window of $\Delta V_{M(max)} \approx 8.6$ V. However, the ΔV_{Dirac} suddenly reduces after $V_E \approx -24$ V. This is attributed to the electron back-injection from the ITO gate to the charge trap layer *via* Fowler-Nordheim tunneling (Figure 4c). When a negative erase voltage is applied, the charge trap layer is filled with holes and the back injected electrons compensate the overall positively stored charges, resulting in a reduction of ΔV_{Dirac}. To further investigate the transport mechanism of the device, we measure the gate tunneling current of the GCTM. As shown in Figure 4b, the parabolic dependence shows trap-assisted (TA) tunneling[39] as the normal write/erase mechanism, whereas the linear relation below $V_E \approx -24$ V indicates Fowler–Nordheim (FN) tunneling[39,40] to be responsible for the electron back-injection. To suppress or eliminate such effects, a high work-function gate material would be favorable because it will modify the flat band condition and increase the tunneling barrier of the control oxide layer making it difficult for the back-injection to occur.[20] In addition to the large memory window, the GCTM shows 30% data retention per 10 years at room temperature (Figure 4d). At elevated temperatures, the retention characteristics degrade. We noticed that the PEN substrate thermally expands at 85 °C. One possibility of such meager retention is the quality of the tunnel oxide formed at low temperatures. Since the glass transition temperature of the PEN substrate is ~200 °C, we carried out all of the fabrication steps below 110 °C. This might cause the formation of point defects in

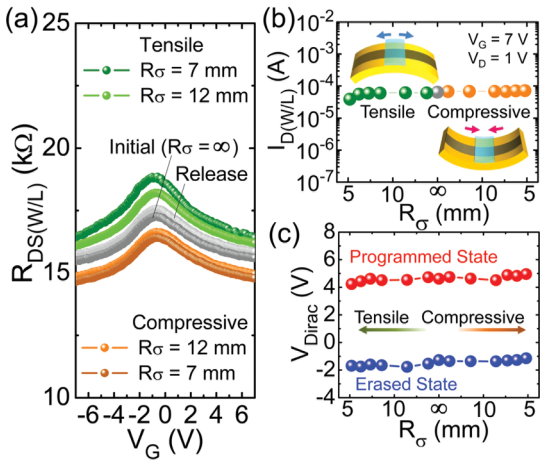

Figure 5. Endurance of electrical characteristics in air under flex. (a) Normalized resistance *vs* gate voltage under tensile and compressive stress at V_D = 1 V. The GCTM reveals minimal Dirac point shift and channel transconductance change under bending. (b) On-state current under bending stress measured at V_D = 1 V and V_G = 7 V. (c) Position of Dirac point under bending stress at program/erase states (V_P = 23 V, V_E = −21 V). For flexures below 7 mm bending curvature, the device remains unchanged after more than 10 cycles.

the tunnel oxide layer and diminish the retention characteristics. Thus, optimizing the process to achieve high quality tunnel oxides at low temperature would be vital to improve the retention characteristics.

Flexible electronics require its functions to sustain under geometric deformation. They will need to be rolled or folded to maximize portability and wearability. The extremely large intrinsic breaking strength of 130 GPa makes graphene resilient to fracture upon stress.[41] On the other hand, the high Young's modulus of graphene (~1 TPa) is sought to be undesirable for deformation, but the atomic thinness makes graphene an exception.[42,43] In some sense, the flexibility of graphene stems from similar reasons to why graphene exhibits a negative thermal expansion coefficient.[44−46] Figure 5a displays the response of normalized resistance ($R_{DS(W/L)} - V_G$) under flex. Since the channel dimension (i.e., overlap region between gate oxide and graphene) is $W/L \approx 4.5\ \mu m/30\ \mu m$, the stress effect would be pronounced along the L direction. Thus, we performed the effect of bending stress along the channel direction. The asymmetric device structure along its vertical direction makes it worthwhile to investigate the impact of both tensile and compressive stress (R_σ: bending radius). The GCTM shows no change in the position of the Dirac point, which suggests the potential profile of the energy bands along the gate electrode and dielectric are stable under bending. Furthermore, no significant change in the slope at the linear regime indicates that the graphene channel is robust under stress. From the channel transconductance ($g_m \propto \mu$), the average electron/hole mobility (μ) of multiple devices is estimated to be ~67 $cm^2/(V \cdot s)$ and varied up to 10% under flex. The slight change in resistance might be due to the contact regions, which requires further investigation.[47] As a consequence, as shown in Figure 5b and 5c, the on-state current measured at V_D = 1 V and V_G = 7 V remains steady, while the Dirac point at the program (V_P = 23 V) and erase (V_E = −21 V) states stays unaffected. Here, we note that ITO is not a highly flexible material; that is, ITO can sustain up to 2.5% of strain without affecting its conductance.[48] Thus, replacing ITO with graphene or transparent-conducting organic materials (*e.g.*, PEDOT:PSS) as the gate electrode would be beneficial to further improve the flexibility of GCTM.

The ON/OFF ratio of graphene-based devices is still an ongoing challenge in the graphene community. Several methods have been proposed to create an energy bandgap in this otherwise gapless material. For example, graphene nanoribbons show that a bandgap of ≤50 meV can be achieved through quantum confinement effects,[49] and bi or trilayer graphene exhibits a bandgap of ≤250 meV under high electric fields.[50,51] In addition, very recently, the usage of Schottky source/drain contacts have shown to improve the ON/OFF ratio of graphene transistors.[30] Implementing such behaviors in our device structure should be the next step to improve the memory performance of graphene-based charge trap flash memory structures.

The operating speed of our graphene charge trap memory would be limited by the capacitive charging speed of the gate stack, since the high graphene mobility[52,53] of 5000 to 100 000 $cm^2/(V\ s)$ renders an extremely short transit time. Therefore, the GCTM structure will have similar operating speeds as the standard charge trap memories, which currently show ~14 ns read time and 20 μs/20 ms write/erase time.[54]

CONCLUSION

The covalently bonded graphene greatly reduces the heat budget and enables fabrication of ultrahigh density transparent-flexible GCTM. The GCTM only reduces 8% of transparency from the PEN substrate and demonstrates memory functionality of 8.6 V memory window with reasonable retention characteristics. Furthermore, the electrical characteristics of the transparent-flexible GCTM exhibit minimal perturbation due to the bending stress. We believe that graphene-based electronic modules will help bring future electronics a step closer to transparent-flexible electronics.

MATERIALS AND METHODS

Graphene Growth and Transfer. The CVD graphene was prepared by depositing a Cu thin film of 500 nm thickness, using electron-beam evaporation, on a SiO_2/Si wafer and placed in an inductively coupled plasma enhanced CVD (PECVD) chamber. The substrate temperature was increased to 650 °C at a base

pressure of 5×10^{-7} Torr and hydrogen plasma was applied for a surface treatment at 650 °C. The monolayer graphene was then grown under an Ar + C_2H_2 gas plasma mixture at 50 mTorr for 3 min. The as-grown graphene film was then transferred to the PET film after removal from the Cu/SiO_2/Si wafer. A spin-coated polymethylmethacrylate (PMMA) and adhesive ultraviolet-tape was placed over the graphene as a protective layer. After peeling the Cu/graphene/PMMA/tape from the growth substrate, the Cu thin film was removed in a dilute $FeCl_3$ solution and the remains were transferred onto the PET substrate. Then, the PMMA and tape were removed by organic solvents.

Electrical and Transmittance Measurements. The electrical characteristics were measured through a semiconductor analyzer (Keithley 4200) under ambient conditions, and the radius of curvature was measured by a stylus profiler. The optical transmittance was taken by a UV−vis−NIR spectrometer (Ocean Optics 2000).

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. This work was supported by the Focus Center Research Program (FCRP)−Functional Engineered Nano Architectonics (FENA) and the NSF IGERT Materials Creation Training Program Grant DGE-11443. The work at The Aerospace Corporation was supported under its Independent Research and Development program.

Supporting Information Available: This section includes the Raman characteristics of SLG and the quantitative representation of the energy band diagram for GCTM. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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